

1                   CLAIMS:

2                   1. A field effect transistor comprising:  
3                   a pair of source/drain regions having a channel region positioned  
4                   therebetween; and  
5                   a gate positioned operatively proximate the channel region, the  
6                   gate comprising conductively doped semiconductive material, a silicide  
7                   layer and a conductive diffusion barrier layer.

8

9                   2. The transistor of claim 1 wherein the conductive diffusion  
10                  barrier layer is in contact with the semiconductive material.

11

12                  3. The transistor of claim 1 wherein the conductive diffusion  
13                  barrier layer is not in contact with the semiconductive material.

14

15                  4. The transistor of claim 1 wherein the conductive diffusion  
16                  barrier layer is in contact with the silicide layer.

17

18                  5. The transistor of claim 1 wherein the conductive diffusion  
19                  barrier layer is in contact with both the semiconductive material and the  
20                  silicide layer.

21

22                  6. The transistor of claim 1 wherein the conductive diffusion  
23                  barrier layer is received over the semiconductive material.

24

1           7. The transistor of claim 1 wherein the conductive diffusion  
2           barrier layer is received over the silicide layer.

3  
4           8. The transistor of claim 1 wherein the conductive diffusion  
5           barrier layer is received over both the semiconductive material and the  
6           silicide layer.

7  
8           9. The transistor of claim 1 wherein the silicide layer is  
9           received over the conductive diffusion barrier layer.

10  
11          10. The transistor of claim 1 wherein the conductive diffusion  
12          barrier layer comprises  $W_xN_y$ .

13  
14          11. The transistor of claim 1 wherein the conductive diffusion  
15          barrier layer comprises titanium.

16  
17          12. The transistor of claim 11 wherein the conductive diffusion  
18          barrier layer is selected from the group consisting of  $TiN$ ,  $TiO_xN_y$ , and  
19           $TiW_xN_y$ , and mixtures thereof.

20  
21          22. The transistor of claim 1 wherein the conductively doped  
22          semiconductive material comprises n+ polysilicon.

1           14. The transistor of claim 1 wherein the conductively doped  
2           semiconductive material comprises p+ polysilicon.

4           15. The transistor of claim 1 wherein the silicide layer and the  
5           conductive diffusion barrier layer comprise the same metal.

7           16. Integrated circuitry comprising:

8           a field effect transistor including a gate, a gate dielectric layer,  
9           source/drain regions and a channel region; the gate comprising  
10          semiconductive material conductively doped with a conductivity enhancing  
11          impurity of a first type and a conductive diffusion barrier layer; and

12          insulative material received proximate the gate, the insulative  
13          material including semiconductive material provided therein in electrical  
14          connection with the gate, the semiconductive material provided within  
15          the insulative material being conductively doped with a conductivity  
16          enhancing impurity of a second type, the conductive diffusion barrier  
17          layer of the gate being provided between the gate semiconductive  
18          material and the semiconductive material provided within the insulative  
19          material.

21           17. The integrated circuitry of claim 16 wherein the first type  
22          is n and the second type is p.

1           18. The integrated circuitry of claim 16 wherein the first type  
2           is p and the second type is n.

3  
4           19. The integrated circuitry of claim 16 wherein the gate also  
5           comprises a conductive silicide.

6  
7           20. The transistor of claim 19 wherein the silicide and the  
8           conductive diffusion barrier layer comprise the same metal.

9  
10          21. The integrated circuitry of claim 16 wherein the  
11          semiconductive material within the insulating material contacts the  
12          conductive diffusion barrier layer of the gate.

13  
14          22. The integrated circuitry of claim 16 wherein the  
15          semiconductive material within the insulating material does not contact  
16          the conductive diffusion barrier layer of the gate.

17  
18          23. The integrated circuitry of claim 16 wherein the gate also  
19          comprises a conductive silicide, the semiconductive material within the  
20          insulating material contacting the silicide.

1           24. The integrated circuitry of claim 16 wherein the conductive  
2 diffusion barrier layer is received over the gate semiconductive material,  
3 and the semiconductive material within the insulating material is received  
4 over the gate.

5  
6           25. The integrated circuitry of claim 16 wherein the insulative  
7 material comprises an opening within which the semiconductive material  
8 therein has been provided, the opening being substantially void of any  
9 conductive diffusion barrier layer material.

10  
11          26. A method of forming a field effect transistor gate  
12 comprising:

13           forming a layer of conductively doped semiconductive material over  
14 a substrate;

15           forming a layer of a conductive silicide over the substrate;

16           forming a conductive diffusion barrier layer over the substrate; and  
17           removing portions of the semiconductive material layer, the silicide  
18 layer and the conductive diffusion barrier layer to form a transistor gate  
19 comprising the semiconductive material, the conductive silicide and the  
20 conductive diffusion barrier layer.

21  
22          27. The transistor of claim 26 wherein the silicide layer and the  
23 conductive diffusion barrier layer comprise the same metal.

1                   28. The method of claim 26 wherein the removing comprises:  
2                   forming a masking layer over the semiconductive material, the  
3                   conductive silicide layer and the conductive diffusion barrier layer and  
4                   leaving said portions unmasked by the masking layer; and  
5                   etching away the unmasked portions to form the transistor gate  
6                   beneath the masking layer.

7  
8                   29. The method of claim 26 wherein the removing comprises:  
9                   depositing, selectively light exposing and developing a layer of  
10                  photoresist to form a photoresist mask over the semiconductive material,  
11                  the conductive silicide layer and the conductive diffusion barrier layer  
12                  and leaving said portions unmasked by the photoresist; and  
13                  etching away the unmasked portions to form the transistor gate  
14                  beneath the photoresist.

15  
16                  30. The method of claim 26 comprising providing the conductive  
17                  diffusion barrier layer in contact with the semiconductive material layer.

18  
19                  31. The method of claim 26 comprising forming the conductive  
20                  diffusion barrier layer after and in contact with the semiconductive  
21                  material layer.

1           32. The method of claim 26 comprising forming the conductive  
2 diffusion barrier layer after and not in contact with the semiconductive  
3 material layer.

4  
5           33. The method of claim 26 comprising providing the conductive  
6 diffusion barrier layer in contact with the silicide layer.

7  
8           34. The method of claim 26 providing the conductive diffusion  
9 barrier layer in contact with both the semiconductive material layer and  
10 the silicide layer.

11  
12          35. The method of claim 26 comprising forming the conductive  
13 diffusion barrier layer over the semiconductive material layer.

14  
15          36. The method of claim 26 comprising forming the conductive  
16 diffusion barrier layer over the silicide layer.

17  
18          37. The method of claim 26 comprising forming the conductive  
19 diffusion barrier layer over both the semiconductive material layer and  
20 the silicide layer.

21  
22          38. The method of claim 26 comprising forming the silicide layer  
23 over the conductive diffusion barrier layer.

1                   39. The method of claim 26 comprising forming the conductive  
2                   diffusion barrier layer to be selected from the group consisting of TiN,  
3                    $TiO_xN_y$ ,  $W_xN_y$  and  $TiW_xN_y$ , and mixtures thereof.

4  
5                   40. A method of forming integrated circuitry comprising:  
6                   forming a field effect transistor gate over a substrate, the gate  
7                   comprising semiconductive material conductively doped with a conductivity  
8                   enhancing impurity of a first type and a conductive diffusion barrier  
9                   layer;

10                  forming an insulative layer over the substrate;  
11                  forming an opening into the insulative layer;  
12                  forming semiconductive material conductively doped with a  
13                  conductivity enhancing impurity of a second type within the opening;  
14                  and

15                  providing the doped semiconductive material within the opening in  
16                  electrical connection with the gate, with the conductive diffusion barrier  
17                  layer of the gate being received between the semiconductive material of  
18                  the gate and the semiconductive material within the opening.

19  
20                  41. The method of claim 40 wherein the first type is n and the  
21                  second type is p.

22  
23                  42. The method of claim 40 wherein the first type is p and the  
24                  second type is n.

1           43. The method of claim 40 comprising forming the gate to also  
2 comprise a conductive silicide.

3  
4           44. The transistor of claim 43 wherein the silicide and the  
5 conductive diffusion barrier layer comprise the same metal.

6  
7           45. The method of claim 40 comprising forming the  
8 semiconductive material within the opening to contact the conductive  
9 diffusion barrier layer of the gate.

10  
11          46. The method of claim 40 wherein the semiconductive material  
12 formed within the opening does not contact the conductive diffusion  
13 barrier layer of the gate.

14  
15          47. The method of claim 40 comprising forming the gate to also  
16 comprises a conductive silicide, the semiconductive material within the  
17 opening contacting the silicide.

18  
19          48. The method of claim 40 wherein the opening is filled with  
20 conductive material none of which comprises any conductive diffusion  
21 barrier layer material.

1                   49. A method of forming integrated circuitry comprising:  
2                   forming a field effect transistor gate over a substrate, the gate  
3                   comprising semiconductive material conductively doped with a conductivity  
4                   enhancing impurity of a first type and a conductive diffusion barrier  
5                   layer received thereover;  
6                   forming an insulative layer over the gate;  
7                   forming an opening into the insulative layer to a conductive  
8                   portion of the gate; and  
9                   forming semiconductive material conductively doped with a  
10                  conductivity enhancing impurity of a second type within the opening in  
11                  electrical connection with the conductive portion, with the conductive  
12                  diffusion barrier layer of the gate being received between the  
13                  semiconductive material of the gate and the semiconductive material  
14                  within the opening.

15  
16                  50. The method of claim 49 wherein the first type is n and the  
17                  second type is p.

18  
19                  51. The method of claim 49 wherein the first type is p and the  
20                  second type is n.

21  
22                  52. The method of claim 49 comprising forming the gate to also  
23                  comprise a conductive silicide.

1           53. The method of claim 49 comprising forming the  
2 semiconductive material within the opening to contact the conductive  
3 diffusion barrier layer of the gate.

4  
5           54. The method of claim 49 wherein the semiconductive material  
6 formed within the opening does not contact the conductive diffusion  
7 barrier layer of the gate.

8  
9           55. The method of claim 49 comprising forming the gate to also  
10 comprises a conductive silicide, the semiconductive material within the  
11 opening contacting the silicide.

12  
13           56. The method of claim 49 wherein the opening is filled with  
14 conductive material none of which comprises any conductive diffusion  
15 barrier layer material.

16  
17           Add 1  
18           Add B8  
19  
20           Add C2  
21  
22  
23  
24